AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows. Please cancel claim 4 without prejudice or disclaimer. Please add new claims 5-19.

1. (Currently Amended) A memory device comprising:

a data memory to and from which image data is input and output via a data bus for [[a]] the data memory; ~~and~~

a plurality of buffer circuits for inputting and outputting image data to and from said data memory via a first data bus that has a bus width the same as that of the data bus for said data memory and that is electrically connected to the data bus for said data memory, and inputting and outputting image data to and from a data processing circuit via a second data bus having a bus width smaller than that of the data bus for said data memory[[.]]; and

an arbitration circuit, which is connected between the data processing circuit and said plurality of buffer circuits, for controlling the plurality of buffer circuits in such a manner that image data representing images of different frames is input and output to and from different buffer circuits in a common time period.

2. (Original) The device according to claim 1, further comprising a selector, which is connected between said plurality of buffer circuits and said data memory, for allowing input/output of data between any one of said plurality of buffer circuits and said data memory.

3. (Original) The device according to claim 1, wherein the bus width of the

second data bus is a fraction of that of the bus for said data memory.

4. (Canceled.)

5. (New) The device according to claim 1, wherein said arbitration circuit operates the data processing circuit and said plurality of buffer circuits directly.

6. (New) The device according to claim 1, wherein the device is devoid of structure between said arbitration circuit and the data processing circuit, and devoid of structure between said arbitration circuit and said plurality of buffer circuits.

7. (New) The device according to claim 1, wherein a time required to write and read image data between the data memory and the plurality of buffer circuits is one-fourth of a time required to write and read image data between the plurality of buffer circuits and the arbitration circuit.

8. (New) The device according to claim 1, further comprising:

an address generating circuit for generating addresses of a destination at which said image data is to be stored, the address generating circuit being connected between the data processing circuit and the arbitration circuit via the second bus.

9. (New) The device according to claim 1, further comprising:

a plurality of address generating circuits for generating addresses of a destination at which said image data is to be stored, the plurality of address generating circuits being

connected between the data processing circuit and the arbitration circuit via the second bus.

10. (New) The device according to claim 9, wherein the plurality of address generating circuits comprise:

a first address generating circuit for inputting image data to the data processing circuit; and

a second address generating circuit for outputting output data generated from the data processing circuit to the arbitration circuit via the second bus.

11. (New) The device according to claim 10, wherein the data processing circuit generates output data comprising luminance data and color difference data.

12. (New) The device according to claim 10, wherein the data processing circuit generates output data comprising image enlarging/reducing data.

13. (New) The device according to claim 10, wherein the data processing circuit generates output data comprising image compressing/expanding data.

14. (New) The device according to claim 8, wherein the data processing circuit generates output data to be written to an external memory device.

15. (New) The device according to claim 1, further comprising:

a charge coupled device (CCD) and from which data is output via the second data bus to the arbitration circuit and the plurality of buffer circuits.

16. (New) The device according to claim 1, further comprising:

a selector circuit for inputting and outputting image data to and from the data memory and the plurality of buffer circuits.

17. (New) The device according to claim 16, further comprising:

a central processor that controls the selector circuit.

18. (New) A method for a memory device, comprising:

providing a data memory to and from which data is input and output via a data bus for the data memory;

electrically connecting a first data bus to the data bus for said data memory, wherein the first data bus width is the same as that of the data bus for said data memory;

providing a plurality of buffer circuits to and from which image data is input to and output from said data memory via the first data bus;

providing a second data bus having a bus width smaller than that of the data bus for said data memory;

providing a data processing circuit to and from which image data is input to and output from via the second data bus; and

connecting an arbitration circuit between the data processing circuit and said plurality of buffer circuits, for controlling the plurality of buffer circuits such that image data representing images of different frames is input to and output from different buffer circuits in a common time period.

19. (New) A memory device, comprising:

means for storing data to and from which said data is input and output via a data bus for the storing means;

a plurality of input/output (I/O) means for inputting and outputting image data to and from said storing means via a first data bus that has a bus width the same as that of the data bus and that is electrically connected to the data bus for said storing means, and inputting and outputting image data to and from a data processing circuit via a second data bus having a bus width smaller than that of the data bus for said storing means; and

means, connected between the data processing circuit and said plurality of I/O means, for controlling the I/O means for inputting and outputting such that image data representing images of different frames is input and output to and from different I/O means in a common time period.